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September 29, 2003

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

TRANSMITTAL SHEET

Applicant: James John Casto, et al.
Title: INTEGRATED CIRCUIT PACKAGE INCORPORATING PROGRAMMABLE ELEMENTS
Application No.: 09/484,311 Filed: January 18, 2000
Atty. Docket No.: 1001-0087 Client Ref. No.: TT3309

Dear Sir:

Transmitted herewith are the following documents in the above-identified application:

- ☐ Response to Non-Final Action (page(s))
- ☐ Petition for Extension of Time (month) (page(s))
- ☐ Information Disclosure Statement (page(s)), including PTO Form 1449 (page(s)), and copies of reference(s)
- ☒ Other: Appellants' Brief (21 page(s)) in triplicate;
- ☐ Other: (page(s))
- ☐ Other: (page(s))
- ☒ A Return Postcard and this Transmittal Letter (2 pages), in duplicate

The Total Fee has been calculated as shown below:

	Claims After Amendment	Claims Previously Paid	Extra Claims	Fees
Total Claims	N/A	– 20 =	0 x $18.00 =	0.00
Independent Claims		– 3 =	0 x $84.00 =	0.00
Multiple Dependent Claims (if any) - $280.00 fee				
Additional Claims Fee				$ .00
Fee For Extension Of Time				
Other Fees: (Appeal Brief)				320.00
TOTAL FEE DUE:				$ 320.00

- ☐ Applicant is, or has established status as, a small entity.
- ☐ A check is enclosed for the Total Fee shown above.
- ☒ Please charge the Total Fee shown above to Deposit Account 01-0365.
- ☒ The Commissioner is hereby authorized to charge any additional fees under 37 C.F.R. § 1.16 or 1.17 which may be required during the pendency of this application, and to similarly credit any overpayment, to Deposit Account 01-0365.

CERTIFICATE OF MAILING OR TRANSMISSION

I hereby certify that, on the date shown below, this correspondence is being

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Nicole Teitler Cave 9/29/03
Date

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Respectfully submitted,

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PATENT

#19 Appeal Brief 4 Pokman 10/17/03

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s):	James John Casto, et al.		
Title:	INTEGRATED CIRCUIT PACKAGE INCORPORATING PROGRAMMABLE ELEMENTS		
Application No.:	09/484,311	Filed:	1/18/00
Examiner:	E. Lee	Group Art Unit:	2815
Atty. Docket No.:	1001-0087	Confirmation No.:	9539

September 29, 2003

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APPELLANTS' BRIEF (37 C.F.R. § 1.192)

This brief is in furtherance of the Notice of Appeal, filed on July 31, 2003. The fees required under § 1.17(c), are provided in the accompanying Transmittal. This brief is being transmitted in triplicate pursuant to 37 C.F.R. § 1.192(a).

REAL PARTY IN INTEREST

The real party in interest in this appeal is Advanced Micro Devices, Inc.

RELATED APPEALS AND INTERFERENCES

Appellants have no knowledge of any related appeals or interferences.

STATUS OF CLAIMS

Claims 2-12, 15-25, and 27 are presented herein on appeal. Claims 1-38 were originally presented. Claims 28-36 were withdrawn from consideration in response to a restriction requirement. Claims 1, 14, 26, and 37-38 were cancelled in response to a first Office Action. Claim 13 was cancelled in response to a second Office Action.

Claims 2-12, 15-25, and 27, now presented herein on appeal are reproduced in the Appendix attached hereto.

STATUS OF AMENDMENTS

No amendment after final rejection has been filed.

SUMMARY OF INVENTION

Referring to Fig. 2, an overview of a system incorporating one embodiment of the present invention is illustrated. Fig. 2 shows microprocessor 201 which includes package 203 that holds integrated circuit die (also commonly referred to as chip) 205. Package 203 includes fuses 207. Based on the programming of fuses 207, the package supplies voltage regulator 209 with VID signals 211. Based on the VID signals, voltage regulator 209 supplies core voltage 212 to processor 201. In addition, the package may supply system controller 213 (e.g. a north bridge including a memory controller and a PCI bridge) with frequency ID signals 215 which indicate the system clock multiplier at which the processor core operates. The fuses may also supply one or more parameters to chip 205.

Package 203 includes a number of external connections such as those providing VID signals 211. Note that the term package as used herein is intended to include any integrated circuit carrier. The exact nature of the external connection between the package and the card to which it attaches, e.g., a motherboard or daughter card, varies according to the type of package. In addition to the external connections, the package provides connections between chip 205 and package 207. The connection between chip and package varies according to the type of package. The connections between the package and the chip and the package and the board provide for signal input/output (I/O), which convey signal information to and from the integrated circuit chip. In addition to signal I/O, the package connections provide connections for Vss and Vcc. A wide variety of package technologies exist that can exploit the present invention. The packages are typically multi-layered packages with vias providing interconnections between the various layers.

As shown in Fig. 2, fuses specifying operating parameters such as voltage may be formed on the surface of the package. The fuses may be formed by a metallization pattern on the package surface that connect through vias to other layers of the multi-layer package and subsequently to interconnections between the chip and package, external package connections, or both.

A laser process (e.g., using a CO2, UV or a diode pumped Nd:YAG laser) may be used to program the fuses by ablating away a portion of the metallization pattern once the appropriate setting(s) for the fuse or array of fuses are known. By programming an array of fuses, the appropriate "data" for operating the processor (e.g., voltage or frequency control values) may be specified. The fuse area on the package can then be covered with a suitable insulating material to prevent later tampering or accidental damage.

Figs. 3A - 3C illustrate various programming possibilities for exemplary fuses. The fuses are formed by metal traces, or other suitable conductors, which connect to vias, indicated by dark circles at each end of the fuse. The vias shown, in general connect to package pins (i.e. external package connections), package power supply nodes (Vss or Vcc) or internal package nodes that connect to the integrated circuit die when it is mounted on the package. The particular connection depends on the type of information intended to be specified by the fuses. Figure 3A shows the fuses prior to programming.

The fuses shown in Fig. 3A determine four bits of information. Each bit requires at least one cut. As shown in Fig. 3A, the top row of fuses 301-304 couple through vias 306-309 to Vcc. The top row of fuses also connect to vias 310-313, which in turn are coupled to package pins to provide four VID bits for connection to a voltage regulator. The bottom row of fuses 315-318 couple at one end through vias 320-323 to Vss. At the other end, the fuses couple to vias 310-313 and thus connect to one end to the top row of fuses 301-304.

Each of the fuses 301-304 and 315-318 include a fusible link coupling each end of the fuse formed by the metal trace or other suitable conductor. Referring to Fig. 3B, the programming shown provides a binary setting of 1-0-0-1 as the value of the fuses, where 1 is Vcc and 0 is Vss. That is, fuses 315 and 317 are blown causing vias 310 and 312 to be coupled

only to Vcc. Fuses 302 and 304 are also blown causing vias 311 and 313 to be only coupled to Vss.

In addition to the four package pins required in Figs. 3A and 3B and the three package pins required in Fig. 3C, an additional package pin may be required in order to provide a special Vcc pin for testing purposes. Otherwise, the package may have its Vcc and Vss planes shorted together during package and integrated circuit testing prior to programming of the fuses.

Note that the use of the term "package pin" is used herein for convenience in describing certain embodiments. While the term is used herein to sometimes describe pins of PGA packages, the term is also used generally herein and is intended to encompass any external connection or contact between the package and the board.

Rather than provide fuse pairs to determine each VID value as illustrated in Figs. 3A-3C, alternatively a single fuse can be used to selectively couple a package pin to a power supply voltage. For example, referring to Fig. 4A, the values for VID are provided by fuses 401-404. Each bit requires at most one cut. Fuses 401-404 couple through vias 406-409 to external package connections and provide, e.g., four VID bits for connection to a voltage regulator. The fuses also connect to vias 410-413, which in turn are coupled to Vss.

If fuse 401 is blown, then the package pin is not connected to Vss. An external pull-up circuit is required to set the package pin to Vcc (unless the receiving circuit can distinguish a float from a ground). Fig. 4B shows another representation of the fuses shown in Fig. 4A. Each of the fuses shown in Figs. 4A and 4B is represented by the circuit shown in Fig. 5, which shows fuse 501 coupled to Vss through a low resistance resistor 502 (0 ohms is acceptable) and to package pin 503. The configuration shown in Fig. 4 requires a maximum of only one cut per bit of information but does require external pull-up circuits. The minimum number of cuts for four bits of information is 0 while the maximum number of cuts is four. With the four fuses shown in Figs. 3A or 4A, up to sixteen different voltage ID values may be specified. Cut here refers to blowing the fuse, typically using a laser, although other methods are possible as described further herein.

While the power supply voltage on the package shown in the embodiment in Figs. 4A and 4B is Vss, it is of course possible to instead provide a one-time programmable connection to Vcc on the package and have an external pull down circuit.

Other parameters may also be specified rather than voltage. For example, as described with relation to Fig. 2, frequency ID information may also be specified.

Referring to Fig. 6, another fuse configuration is illustrated which provides four bits of information. The fuses are again configured in pairs (e.g., fuses 601 and 602) in a manner similar to Figs. 3A-3C. The top fuses 601, 603, 605 and 607 of each pair couple to Vcc through resistors in resistor pack 610. The bottom fuse of each fuse pair, fuses 602, 604, 606 and 608, couple to Vss through resistors in resistor pack 612. The resistors provide a voltage divider function and thus, an extra test pin (to avoid having Vss shorted to Vcc during testing prior to programming of the fuses) may not be necessary. In the embodiment shown in Fig. 6, each of the fuse pairs couple respectively to common nodes 614-617. The common nodes 614-617 couple to external package connections, e.g., package pins. In other embodiments, the common nodes may couple only to external package connections (package pins) or only to the chip and not utilize package pins.

Fig. 7 illustrates an embodiment in which the value specified by the fuse array is provided to the integrated circuit instead of going to the package pins. Internal nodes 614-617 couple to, e.g., C4 pads coupling the die to the package. The fuse array may be specifying a voltage, frequency or other parameter to the integrated circuit die.

Fig. 8 illustrates an embodiment in which fuse elements 624-627 are coupled serially between common nodes 614-617 and external package pins 620-623. The fuses 624-627 can be used in testing environments, where for example, an internal signal must be accessible during test but is then decoupled from the package pin by blowing the fuse prior to product shipment. Fig. 9 illustrates an embodiment combining the various embodiments illustrated in Figs. 6-8. A schematic of one of the fuse pairs in Fig. 6-9 is shown in Fig. 10.

In order to program the fuse configuration shown in Figs. 6-10, at least one fuse of each pair must be blown to connect the common node to either Vcc or Vss. Thus, for four bits of

information, four cuts are generally required. If three state logic is available then both fuses of a pair can be cut to represent a third value.

Referring to Fig. 11 another embodiment illustrates a fuse, without the voltage divider configuration used in Figs. 6-10, providing a parameter value to the integrated circuit die mounted on the package. In the particular embodiment, a signal is provided to that selectively enables error correcting code (ECC) according to the state of the fuse. The ECC signal may be used, e.g., for an on-board cache for a microprocessor. An internal pull-up is required in the processor to specify a value if the fuse is not cut.

The description so far has described cutting fuses with lasers. Several alternative embodiments are also possible. For instance, while the fuses have been described as being laser programmable, the fusible links may also be programmed electrically in a manner known in the art. That is the fuses may be fabricated as electrically programmable fuses. Further, while the fuses have been described as being on the surface of the package, the fuses may actually be fabricated on internal layers of a multi-layer package and be fabricated out of a conductive material other than metal. If fuses are on a layer other than the surface of the package, then electrically programmable fuses may be preferred.

One advantage of the present invention is that the testing procedures to characterize the part may be completed prior to programming of the fuses. Thus, the part in question may complete tests on automatic test equipment (ATE) as well as system level tests. Once the tests are completed and the part is characterized in terms of voltage and speed, the package may be programmed without having to perform any further processing steps on the die or any further testing, except to check that the fuses were appropriately programmed. Of course, the fuses may be programmed prior to mounting the die if the values for the fuses are known.

ISSUES

The Issues on Appeal are:

1. whether Appellants' claims 2-5, 10, 11, 17, 18, 22, and 23 are unpatentable under 35 U.S.C. § 102(e) over MacPherson et al.

2. whether Appellants' claims 2, 7-9, 11, 12, 15-18, 20-23, and 27 are unpatentable under 35 U.S.C. § 102(b) over Crafts et al.

3. whether Appellants' claim 12 is unpatentable under 35 U.S.C. § 102(b) over Hamdy et al.

4. whether Appellants' claim 21 is unpatentable under 35 U.S.C. § 102(b) over Best.

5. whether Appellants' claim 19 and 24 are unpatentable under 35 U.S.C. § 103(a) over MacPherson et al. in view of Hall.

6. whether Appellants' claim 25 is unpatentable under 35 U.S.C. § 103(a) over MacPherson et al. in view of Barth, Jr. et al.

GROUPING OF CLAIMS

Appealed claims 2-12, 15-25, and 27 do not stand or fall together. The claims are grouped as follows:

Group I: claims 2, 5, 6, 8, 9, 10, 11, and 15-16.

Group II: claims 17, 18, 20, 22, 23, and 27.

Group III: claim 3

Group IV: claim 4

Group V: claim 12

Group VI: claim 19

Group VII: claim 21

Group VIII: claim 24

Group IX: claim 25

ARGUMENTS

Claims Group I

Referring to the first group of claims, these claims have been rejected under 35 U.S.C. § 102(e) over MacPherson et al. and under 35 U.S.C. § 102(b) over Crafts et al. For purposes of this discussion, claim 2 of Group I will be addressed. Claim 2 recites a package including at least one pair of programmable elements. The Final Office Action, dated April 7, 2003, refers to Fig. 1 of Macpherson, which teaches a conventional fuse array within an integrated circuit device. (Col. 4, lines 6-9). Because a package is distinct from an integrated circuit device, fuses in the device, taught by MacPherson, fail to teach the claimed package having a pair of programmable elements. Accordingly, Applicants respectfully submit that claim 2 and all claims dependent thereon are patentably distinguishable over MacPherson.

The Final Office Action responded to arguments previously presented by Applicants by pointing out that MacPherson states (col. 1, lines 46, col. 2, line 32) that integrated circuit devices such as PALs, FPGAs, and PLDs are programmed as packaged units or after installation onto a circuit board. Therefore, the Final Office Action argued that Macpherson discloses an integrated circuit wherein the integrated circuit is part of a package and therefore it does not matter whether a package is distinct from a semiconductor. MacPherson teaches at col. 1, lines 46-51 that PALs, FPGAs, and PLDs are fabricated and programmed after they are packaged units. However, MacPherson distinguishes between a device and a package. For example, MacPherson teaches at col. 2, lines 5-7 that "the fuses in the device which define how the circuit is configured are accessed through the I/O pins on the device package." Applicants respectfully submit that a package is distinct from a semiconductor and respectfully request that the appropriate consideration is given to that distinction.

As pointed out previously, Applicants distinguish between the device and the package. For example, the Applicants provide a definition in the specification at page 6, lines 2-10: "the term package as used herein is intended to include any integrated circuit carrier....In addition to the external connections, the package provides connections between chip 205 and package 207."

The meaning of the term "package" and its distinction from the device may also be obtained from a publicly available glossary. "Dictionaries, encyclopedias and treatises, publicly available at the time the patent is issued, are objective resources that serve as reliable sources of information on the established meanings that would have been attributed to the terms of the claims by those of skill in the art." Texas Digital Sys., Inc. v. Telegenix Inc., 64 USPQ2d 1812, 1818 (Fed. Cir. 2002). In general, an integrated circuit package is "[t]he combined mounting and housing for an integrated circuit; the package protects the integrated circuit and permits external connections to be made to it." MODERN DICTIONARY OF ELECTRONICS, 381 (Rudolf F. Graf ed., Newnes 7th ed. 1999). Based on the aforementioned definitions, a package is distinct from a semiconductor device inside the package.

The Examiner also suggested that the package limitation is not going to be given patentable weight because, "where the claim is drawn to a structure and the portion of the claim following the preamble is a self-contained description of the structure not depending for completeness upon the introductory clause" (citing Kropa v. Robie, 88 USPQ 478 (CCPA 1951)).

Applicants respectfully disagree with the Examiner's application of case law and interpretation of the claims. In general, "[i]f the claim preamble when read in the context of the entire claim, recites limitations of the claim, or, if, the claim preamble is 'necessary to give life, meaning, and vitality' to the claim, then the claim preamble should be construed as if in the balance of the claim" Pitney Bowes, Inc. v. Hewlett-Packard Co., 51 USPQ2d 1161, 1165 (Fed. Cir. 1999) (citing Kropa v. Robie, 88 USPQ 478, 480-81 (CCPA 1951)). "[A] claim preamble has the import that the claim as a whole suggests for it. In other words, when the claim drafter chooses to use *both* the preamble and the body to define the subject matter of the claimed invention, the invention so defined, and not some other, is the one the patent protects." Bell Communications Research, Inc. v. Vitalink Communications Corp., 34 USPQ2d 1816, 1820 (Fed. Cir. 1995). "When limitations in the body of the claim rely upon and derive antecedent basis from the preamble, then the preamble may act as a necessary component of the claimed invention." See Eaton Corp. v. Rockwell Int'l Corp., 66 USPQ2d 1271, 1276 (2003).

Referring to claim 2, the plain language of the body of the claim explicitly refers to and defines the package structure ("power supply voltage node in the package", "being coupled through an internal package node"). When the body of the claim refers to "the package", it is referring back to the particular package previously described in the preamble. Thus, it is clear that the preamble language referring to the package and the additional references to structural limitations of the package clearly require that "package" be given weight.

Regarding the rejection over Crafts, the Final Office Action pointed to Fig. 3 of Crafts. Fig. 3 is a schematic diagram of a fuse array PROM. (Col. 2, lines 61-62). Crafts teaches a programmable read only memory (PROM) including an array of polysilicon fuse elements formed within a semiconductor substrate. See Abstract. Crafts fails to teach a package that includes at least one pair of programmable elements, the one pair including a one-time programmable element and a second one-time programmable element, the second one-time programmable element having a first and second end, the first end of the second one-time programmable element coupled to a second power supply voltage node and the second end of the second one-time programmable element being coupled through an internal package node to the second end of the first one-time programmable element as required by claim 2. Even if memory devices are formed in dies in semiconductor packages, as the Examiner suggested, a PROM device and a fuse array structure for implementation within an integrated circuit, as taught by Crafts, fails to teach programmable elements as recited by claim 2. Accordingly, Applicants respectfully submit that the claim 2 distinguishes over Crafts.

For at least these reasons, the PTO's rejections of claim 2 and all claims of Group 1, should be reversed.

Claims Group II

Referring to the second group of claims, these claims have been rejected under 35 U.S.C. § 102(e) over MacPherson et al. and under 35 U.S.C. § 102(b) over Crafts et al. For purposes of this discussion, claim 17 of Group II will be addressed. Claim 17 recites a package including one or more one-time programmable elements. The Final Office Action, dated April 7, 2003, refers to Fig. 1 of Macpherson, which teaches a conventional fuse array within an integrated circuit device. (Col. 4, lines 6-9). Because a package is distinct from an integrated circuit

device, fuses in the device, taught by MacPherson, fail to teach the claimed package having one or more one-time programmable elements. Accordingly, Applicants respectfully submit that claim 17 and all claims dependent thereon are patentably distinguishable over MacPherson.

The Final Office Action responded to arguments previously presented by Applicants by pointing out that MacPherson states (col. 1, lines 46, col. 2, line 32) that integrated circuit devices such as PALs, FPGAs, and PLDs are programmed as packaged units or after installation onto a circuit board. Therefore, the Final Office Action argued that Macpherson discloses an integrated circuit wherein the integrated circuit is part of a package and therefore it does not matter whether a package is distinct from a semiconductor. MacPherson teaches at col. 1, lines 46-51 that PALs, FPGAs, and PLDs are fabricated and programmed after they are packaged units. However, MacPherson distinguishes between a device and a package. For example, MacPherson teaches at col. 2, lines 5-7 that "the fuses in the device which define how the circuit is configured are accessed through the I/O pins on the device package." Applicants respectfully submit that a package is distinct from a semiconductor and respectfully request that the appropriate consideration is given to that distinction.

As pointed out previously, Applicants distinguish between the device and the package. For example, the Applicants provide a definition in the specification at page 6, lines 2-10: "the term package as used herein is intended to include any integrated circuit carrier....In addition to the external connections, the package provides connections between chip 205 and package 207."

The meaning of the term "package" and its distinction from the device may also be obtained from a publicly available glossary. "Dictionaries, encyclopedias and treatises, publicly available at the time the patent is issued, are objective resources that serve as reliable sources of information on the established meanings that would have been attributed to the terms of the claims by those of skill in the art." Texas Digital Sys., Inc. v. Telegenix Inc., 64 USPQ2d 1812, 1818 (Fed. Cir. 2002). In general, an integrated circuit package is "[t]he combined mounting and housing for an integrated circuit; the package protects the integrated circuit and permits external connections to be made to it." MODERN DICTIONARY OF ELECTRONICS, 381 (Rudolf F. Graf ed., Newnes 7th ed. 1999). Based on the aforementioned definitions, a package is distinct from a semiconductor device inside the package.

Regarding the rejection over Crafts, the Final Office Action pointed to Fig. 3 of Crafts. Fig. 3 is a schematic diagram of a fuse array PROM. (Col. 2, lines 61-62). Crafts teaches a programmable read only memory (PROM) including an array of polysilicon fuse elements formed within a semiconductor substrate. See Abstract. Crafts fails to teach a package including one or more one-time programmable elements having a first and a second end separated by a programmable link, wherein the first end of the one one-time programmable element is coupled to a power supply voltage node in the package and a second end of the programmable link is coupled to an internal package node, as required by claim 17. Even if memory devices are formed in dies in semiconductor packages, as the Examiner suggested, a PROM device and a fuse array structure for implementation within an integrated circuit, as taught by Crafts, fails to teach programmable elements as recited by claim 17. Accordingly, Applicants respectfully submit that the claim 17 distinguishes over Crafts.

For at least these reasons, the PTO's rejections of claim 17 and all claims of Group II, should be reversed.

Claims Group III

Referring to the third group of claims, claim 3 has been rejected under 35 U.S.C. § 102(e) over MacPherson et al. Claim 3 further defines the package structure by reciting a multilayered package and that the programmable element is formed of a metallization pattern located on the surface of the package. With respect to claim 3, Applicants respectfully submit that MacPherson nowhere teaches a multilayered package and that the programmable element is formed of a metallization pattern located on the surface of the package. Clearly, this claim is directed towards the package structure and such limitations are not taught by MacPherson's semiconductor device within a package. Thus, the PTO should have given patentable weight to the structural limitations of the package described in claim 3. For at least these reasons, the PTO's rejection of claim 3, the only claim in Group III, should be reversed.

Claims Group IV

Referring to the fourth group of claims, claim 4 has been rejected under 35 U.S.C. § 102(e) over MacPherson et al. Claim 4 recites a multilayered package and that the

programmable element is located on a layer of the package, other than the surface of the package. With respect to claim 3, Applicants respectfully submit that MacPherson nowhere teaches a multilayered package and that the programmable element is formed of a metallization pattern located on other than the surface of the package. Clearly, this claim is directed towards the package structure and such limitations are not taught by MacPherson's semiconductor device within a package. Thus, the PTO should have given patentable weight to the structural limitations of the package described in claim 4. For at least these reasons, the PTO's rejection of claim 4, the only claim in Group IV, should be reversed.

Claims Group V

Referring to the fifth group of claims, claim 12 has been rejected under 35 U.S.C. § 102(b) over Hamdy et al. The Final Office Action points to Fig. 5a. Fig. 5a of Hamdy is a circuit diagram showing an application of the electrically programmable low-impedance anti-fuse of the present invention as a read-only-memory. (Col. 6, lines 32-34). Hamdy teaches that anti-fuses may be formed as a diffusion region in a semiconductor substrate. See Abstract. At col. 3, lines 48-50, Hamdy teaches that "[t]he anti-fuses may be blown either before or after packaging of the integrated circuit die." The semiconductor integrated circuit of Hamdy is distinct from the package recited in claim 12. Claim 12 recites, and Hamdy fails to teach, a package for mounting an integrated circuit die comprising at least one one-time programmable element having a first and a second end separated by a programmable link, wherein the first end of the one-time programmable element is coupled to a power supply voltage node in the package and wherein the package further comprises another programmable element serially coupled between the second end of the programmable element and an external package connection.

Claim 12 recites that another programmable element is serially coupled between the second end of the programmable element and an external package connection. That structure is shown, for example, in Fig. 8 where programmable elements 624-627 are coupled between the second end of programmable element 601-607 and external package connectors. The structure illustrated in Fig. 8 provides, as described on page 10, lines 4-7 of the application, "that the fuses 624-627 can be used in testing environments, where, for example, an internal signal must be accessible during test but is then decoupled from the package pin by blowing a fuse prior to

product shipment." That claimed structure and the advantage referenced above is not taught or suggested in any of the references of record alone or in combination.

Hamdy is directed towards electrically programmable interconnect devices for use in integrated circuits. Hamdy fails to teach anything related to one time programmable elements on packages. The Final Office Action points to elements 168d in Fig. 5a of Hamdy and asserts that element 168h is coupled between a second end of anti-fuse 168d and output 178. According to the Final Office Action, the first end of anti-fuse 168d is coupled to bit line 00 (the power supply). Applicants note that the second end of anti-fuse 168d is coupled either to ground through transistor 166d or is floating if the anti-fuse is not programmed. Thus, the element 168h cannot be coupled between the second end as required by the claim and an external package connection. In view of the above remarks, Applicants submit that claim 12 is in condition for allowance.

The Examiner responded to the Applicants arguments by stating that Hamdy clearly states that the anti-fuses are disposed in an integrated circuit and that the integrated circuit is then packaged. Applicants reiterate that programmable elements inside a semiconductor device do not teach the claimed invention, which is directed to a package. The Examiner further responded to the Applicants by referring to col. 13, lines 17-20 of Hamdy where Hamdy point out that when anti-fuse 168 is programmed it is a short circuit. That is exactly the Applicants point. When anti-fuse 168 is programmed, it is then connected to ground through the transistor and then element 168h cannot be serially coupled between the second end as required by the claim and an external package connection since the second end is coupled to ground. Otherwise anti-fuse 168 is floating. In neither case is element 168h coupled between the second end of anti-fuse 168 and an external package connection.

For at least these reasons, the PTO's rejections of claim 12, the only claim in Group V, should be reversed.

Claims Group VI

Referring to the sixth group of claims, claim 19 has been rejected under 35 U.S.C. § 103(a) over MacPherson et al. in view of Hall. Claim 19 recites that the integrated circuit die

recited in claim 17 includes a processor and the one or more operating parameters recited in claim 17 specify an operating voltage of at least a portion of the processor. MacPherson fails to teach a package including one or more one-time programmable elements as recited in claim 17, on which claim 19 depends. That teaching is not supplied in Hall. Hall teaches strapping options on a circuit board assembly. Thus, Hall fails to teach that the one or more operating parameters specified by one time programmable elements specify an operating voltage for a processor. For at least this reason, the PTO's rejections of claim 19, the only claim in Group VI, should be reversed.

Claims Group VII

Referring to the seventh group of claims, claim 21 has been rejected under 35 U.S.C. § 102(b) over Best. Best teaches fuses in an integrated circuit and fails to teach, as required by claim 21, a package containing one or more one-time programmable elements and an integrated circuit die mounted in the package. Because a package is distinct form an integrated circuit, as discussed above with reference to the MacPherson reference, fuses in the integrated circuit taught by Best fail to teach the claimed package including one or more one-time programmable elements. For at least this reason, the PTO's rejections of claim 21, the only claim in Group VII, should be reversed.

Claims Group VIII

Referring to the eighth group of claims, claim 24 has been rejected under 35 U.S.C. § 103(a) over MacPherson et al. in view of Hall. Claim 24 recites that the one or more programmable elements recited in claim 17, when programmed, specify a control value relating to clock frequency at which the processor operates. MacPherson fails to teach a package including one or more one-time programmable elements as recited in claim 17, on which claim 24 depends. That teaching is not supplied in Hall, which teaches strapping options on a circuit board assembly. Thus, Hall fails to teach that the one or more programmable elements specify a control value relating to clock frequency at which the processor operates. For at least these reasons, the PTO's rejections of claim 24, the only claim in Group VIII, should be reversed.

Claims Group IX

Referring to the ninth group of claims, claim 8 has been rejected under 35 U.S.C. § 103(a) over MacPherson, et al. in view of Barth, Jr. et al. As Applicants explained, MacPherson fails to teach a package including one or more one-time programmable elements as recited in claim 25. That teaching is not supplied in Barth, which teaches a dynamic RAM having on-chip ECC.

In addition, the Final Office Action rejected claim 25 relying on MacPherson and Barth, col. 12, lines 10-34, to teach a semiconductor memory device wherein fuses are programmed to perform an error correction. However, that fails to teach that the claimed programmable element specifies use of ECC for the cache memory on the integrated circuit as claimed in claim 25. Instead Barth teaches using fuses to achieve redundancy by efficiently switching in redundant bit lines. See Summary of the Invention. Barth fails to teach or suggest specifying use of ECC using a programmable element as claimed in claim 25.

For at least these reasons, the PTO's rejections of claim 24, the only claim in Group IX, should be reversed.

CONCLUSION

For at least the foregoing reasons, Appellants' presently claimed invention would not have been anticipated under 35 U.S.C. § 102 nor have been obvious to one of ordinary skill in the art under 35 U.S.C. § 103 over the cited prior art. Accordingly, this Board is respectfully requested to reverse the rejection of claims 2-12, 15-25, and 27 and direct this application to be issued.

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Nicole Teitler Cave 9/29/03

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Respectfully submitted,

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APPENDIX OF CLAIMS INVOLVED IN THE APPEAL

2. A package for mounting at least one integrated circuit die, the package comprising at least one one-time programmable element having a first and a second end separated by a programmable link, wherein the first end of the one-time programmable element is coupled to a power supply voltage node in the package and wherein the programmable element is one of a fuse and an antifuse; and wherein

the package includes at least one pair of programmable elements, the one pair including the one one-time programmable element and a second one-time programmable element, the second one-time programmable element having a first and second end, the first end of the second one-time programmable element coupled to a second power supply voltage node and the second end of the second one-time programmable element being coupled through an internal package node to the second end of the first -one-time programmable element.

3. The package as recited in claim 2 wherein the package is a multilayered package and the programmable element is formed of a metalization pattern located on a surface of the package.

4. The package as recited in claim 2 wherein the package is a multi-layered package and the programmable element is located on a layer other than the surface of the package.

5. The package as recited in claim 2 wherein the programmable element is covered by a protective layer.

6. The package as recited in claim 2 wherein the programmable element is not covered by a protective layer.

7. The package as recited in claim 2 wherein the second end of the programmable element is coupled to at least one of an external package connection and a package contact that

connects to an input terminal of the integrated circuit die, after mounting of the integrated circuit die.

8. The package as recited in claim 2 wherein the programmable element is coupled to the power supply terminal through a resistive element.

9. The package as recited in claim 2 wherein the second end of the programmable element is coupled to an external package connection and to an internal package node that couples to an input terminal of the integrated circuit die when the integrated circuit die is mounted.

10. The package as recited in claim 2 wherein the programmable element is programmable using a laser.

11. The package as recited in claim 2 wherein the programmable element is programmable using an electrical current.

12. A package for mounting at least one integrated circuit die, the package comprising at least one one-time programmable element having a first and a second end separated by a programmable link, wherein the first end of the one-time programmable element is coupled to a power supply voltage node in the package and wherein the package further comprises another programmable element serially coupled between the second end of the programmable element and an external package connection.

15. The package as recited in claim 2 wherein the internal package node is coupled to at least one of an external package connection and an input terminal of the integrated circuit die, after mounting of the integrated circuit die.

16. The package as recited in claim 2 further comprising a first resistive element coupled between the internal package node and the power supply node and a second resistive element coupled between the internal package node and the second power supply node.

17. An electronic device comprising:

a package including one or more one-time programmable elements having a first and a second end separated by a programmable link, wherein the first end of the one one-time programmable element is coupled to a power supply voltage node in the package and a second end of the programmable link is coupled to an internal package node;

at least one integrated circuit die mounted in the package; and

wherein the one one-time programmable element is part of a one-time programmable element pair, the programmable element pair including a second one-time programmable element in addition to the one one-time programmable element, the second programmable element having a first end coupled to the internal package node and a second end coupled to a second power supply voltage.

18. The electronic device as recited in claim 17 wherein the one or more programmable elements specify one or more operating parameters relating to the electronic device.

19. The electronic device as recited in claim 18 wherein the integrated circuit die includes a processor and the one or more operating parameters specify an operating voltage of at least a portion of the processor.

20. The electronic device as recited in claim 17 wherein the internal package node is coupled to at least one of an external package connection and the integrated circuit die.

21. An electronic device comprising:

a package including one or more one-time programmable elements having a first and a second end separated by a programmable link, wherein the first end of the one one-time programmable element is coupled to a power supply voltage node in the package and a second end of the programmable link is coupled to an internal package node;

at least one integrated circuit die mounted in the package; and

wherein the internal package node couples to an external package connection through another one-time programmable element.

22. The electronic device as recited in claim 17 wherein the package is a multilayered package and the programmable element is located on a surface of the package.

23. The electronic device as recited in claim 17 wherein the package is a multi-layered package and the programmable element is located on a layer other than the surface of the package.

24. The electronic device as recited in claim 17 wherein the one or more programmable elements, when programmed, specify a control value relating to clock frequency at which the processor operates.

25. An electronic device comprising:

a package including one or more one-time programmable elements having a first and a second end separated by a programmable link, wherein the first end of the one one-time programmable element is coupled to a power supply voltage node in the package and a second end of the programmable link is coupled to an internal package node; and

at least one integrated circuit die mounted in the package and wherein a state of the programmable element specifies use of error correction code (ECC) for a cache memory on the integrated circuit.

27. The electronic device as recited in claim 17 further comprising a first resistive element coupled respectively between the internal package node and the first power supply node and a second resistive element coupled between the internal package node and the second power supply node, thereby providing a voltage divider when the first power supply node is electrically coupled to the second power supply node through the programmable element pair.